**FIRST SEMESTER 2021-22**

**COURSE HANDOUT**

**Date: 06.09.2021**

In addition to part I (General Handout for all courses appended to the Time table) this portion gives further specific details regarding the course.

## Course No : CS G553

#### **Course Title : Reconfigurable Computing**

**Instructor-in-Charge : Mr. Karri Babu Ravi Teja (Pilani),**

**Dr. Syed Ershad Ahmed and Miss Sharvani Gadgil (Hyderabad)**

**1. Course Description:**

Reconfigurable Computing course primarily deals with the following aspects.

* Reconfigurable computing systems (Fine and coarse grained architectures and technology)
* Design and implementation (Algorithms and steps to implement algorithms to FPGAs)
* Temporal partitioning (Techniques to reconfigure systems over time)
* Temporal placement (Techniques and algorithms to exploit the possibility of partial and dynamic hardware reconfiguration)
* On-line communication (State-of-the-art techniques about how modules can communicate data at run-time)
* Applications (applications benefiting from dynamic hardware reconfiguration and verification using Xilinx System Design tools and Boards).

**2. Scope and Objective of the Course:**

Reconfigurable (adaptive) computing is a novel yet important research field investigating the capability of hardware to adapt to changing computational requirements such as emerging standards, late design changes, and even to changing processing requirements arising at run-time. Reconfigurable computing thus benefits from a) the programmability of software similar to the Von Neumann computer and b) the speed and efficiency of parallel hardware execution.

The purpose of the course reconfigurable computing is to instruct students about the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

**3. Text Books**:

1. Wolf Wayne, *FPGA Based System Design*, Pearson Edu, 2004.

**4. Reference Books:**

1. Scott Hauck, André DeHon, Reconfigurable Computing - The Theory and Practice of FPGA Based Computation, The Morgan Kaufmann Series in Systems on Silicon, 2007.
2. C Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications, Springer, 2007.
3. R Vaidyanathan, Trahan Jerry, Dynamic Reconfiguration: Architectures and Algorithms, L, Kluwer Academic, 2003.
4. Uwe Meyer-Baese, DSP with FPGAs, Springer-Verlag, 2003.
5. Journal papers and Conference publications (will be uploaded in the course website)

**5. Course Plan:**

|  |  |  |
| --- | --- | --- |
| Lecture No. | Learning Objectives | Topics to be covered |
| 01, 02 | Introduction | Introduction application and comparison   * General Purpose Computing * Domain Specific Computing * Application Specific Computing * Reconfigurable Computing |
| 03, 04 | VLSI Technology | Wires, Registers and RAM (self-study assignment)   * Wires and vias * Gate delay vs. wire delay * Registers and RAM |
| 05, 06 | Reconfigurable Computing Hardware | Programmable logic, an overview of   * PLA, PAL, SPLD and CPLD |
| 07 to 12 | Hardware Description Languages and Logic Design | Modeling with HDLs (self study assignment)   * Verilog/VHDL   Combinational Network Delay, Power and Energy Optimization |
| 13 to 15 | Reconfigurable Computing Device | FPGA Architecture, FPGA Fabrics  Configuration   * SRAM Based-FPGAs * Permanently Programmed FPGAs   Programmable I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics, Case Studies (Xilinx, Altera, Microsemi etc). |
| 16,17 | Reconfigurable Computing Architecture | Fine - Grained and Course - Grained Reconfigurable Architecture, Case Studies. |
| 18 to 20 | Programming Reconfigurable Systems | Logic Design Process   * Design * Integration * FPGA Design Flow   Implementation Approaches   * Run Time Reconfiguration (RTR) * Partial Reconfiguration (PR) |
| 21 to 23 | Mapping Designs to Reconfigurable Platform | Logic Implementation for FPGAs, Syntax-Directed Translation  Logic Synthesis   * Two-Level Logic Synthesis * Multi-Level Logic Synthesis   LUT-Based Technology Mapping |
| 24 to 27 | High-Level Synthesis for Reconfigurable Devices (Behavioral Design) | Modeling   * DFG, CFG   Introduction to Binding, Scheduling and Allocation, Temporal Partitioning  Temporal Partitioning Algorithms   * ASAP * ALAP |
| 28 to 30 | Temporal Placement and Routing | Offline and Online Temporal Placement  Routing Cost, Routing-Conscious Placement |
| 31 to 33 | Online Communication | Communication at run-time between modules on the Reconfigurable Device |
| 34,35 | Reconfiguration Management | Multi-Context FPGAs, Introduction to Partial Reconfiguration |
| 36,37 | Security in Modern Reconfigurable Devices | Protecting the FPGA design from common threats, Design security concerns, Secure architecture in FPGAs and SoC FPGAs. |
| 38 to 40 | Applications and Example Case Studies | Image Processing, Signal Processing, Pattern Matching, etc.. |

**6. Evaluation Scheme**:

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| --- | --- | --- | --- | --- |
| **Component** | **Duration** | **Weightage (%)** | **Date & Time** | **Nature of component**  **(Close Book/ Open Book)** |
| Mid-Semester Test | 90 Min. | 30 |  | Open Book |
| Comprehensive Examination | 120 Min. | 35 |  | Open Book |
| Assignments | --- | 25 | Will be announced | Open Book |
| Labs |  | 10 | Will be announced | Open Book |

**7. Chamber Consultation Hour**: Will be announced in the class.

**8. Notices:** The notices shall be put on the Google classroom announcement section. Students please register in the google classroom using your BITS mail ID. Students are expected to check the mails on a regular basis.

**9. Make-up Policy:** Make-up will be given on genuine grounds only. Prior application should be made for seeking the make- up examination.

**10. Note (if any): Regarding Assignments**

1. This course has design assignments using Xilinx Vivado design suite and Xilinx partial reconfiguration tools. Assignments are to be done by the students individually. The design project shall be assigned to group of students where it is expected that all the students contribute equally.
2. Academic honesty is a responsibility of every student and each student shall maintain high levels of honesty and integrity during the class, exam and while solving the assignments. Cheating in any form is strictly prohibited and will be penalized. All students are here by requested not to participate, encourage any form of academic malpractice. In case you have noticed any such activity, you shall report it to the undersigned immediately.

K. Babu Ravi Teja

**Instructor-in-charge**

**Course No. CS G553**